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wherein the first isolation technique and the second isolation technique are different and implemented sequentially.

1 5. (Amended) A system for allowing different types of isolation techniques during  
2 fabrication of a semiconductor device, comprising:  
3 a common substrate having a first portion on which a first isolation technique is  
4 implemented during processing and a second portion on which a second isolation  
5 technique is implemented during processing, wherein the first isolation technique and the  
6 second isolation technique are different and implemented sequentially;  
7 an SRAM device implemented on the first portion of the substrate; and  
8 a flash EPROM device implemented on the second portion of the substrate.

9. (Amended) A semiconductor device comprising:  
a common substrate having a first portion on which an STI isolation technique is  
implemented during processing and a second portion on which a LOCOS isolation  
technique is implemented during processing, wherein the STI isolation technique and the  
LOCOS isolation technique are implemented sequentially;  
an SRAM device implemented on the first portion of the substrate; and  
a flash EPROM device implemented on the second portion of the substrate.